UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/637,840	08/08/2003	Zhongmin Li	14993.31	4352

22913 7590 10/07/2004

WORKMAN NYDEGGER (F/K/A WORKMAN NYDEGGER & SEELEY)
60 EAST SOUTH TEMPLE
1000 EAGLE GATE TOWER
SALT LAKE CITY, UT 84111

EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/637,840	LI ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *38-40* is/are allowed.

6)☒ Claim(s) *1-24 and 28-34* is/are rejected.

7)☒ Claim(s) *25-27 and 35-37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/8/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4, 6, 10, 12, 16-19, 24, 29, and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 depends from claim 2. It is not clear in claim 4 of the cited limitations wherein the ratio of the second ideal resistance to the first ideal resistance is between ninety percent and one hundred and ten percent of the ratio of the second ideal effective length-to-width ratio to the first ideal effective length-to-width ratio because the cited limitations have been cited in claim 2 for the range of between sixty percent and one hundred and fifty percent. Clarification is necessary.

Claim 10 depends from claim 9. It is not clear in claim 10 of the cited limitations wherein the ratio of the third ideal effective length-to-width ratio to the second ideal effective length-to-width ratio is one because the cited limitations have been cited in claim 9 for the range of between ninety percent and one hundred and ten percent. Clarification is necessary.

Claim 16 depends from claim 12. It is not clear in claim 16 of the cited limitations wherein the ratio of the third ideal effective length-to-width ratio to the second ideal effective length-to-width ratio is one because the cited limitations have been cited in

claim 15 for the range of between ninety percent and one hundred and ten percent. Clarification is necessary.

Claim 22 depends from claim 21. It is not clear in claim 22 of the cited limitations wherein the ratio of the third ideal effective length-to-width ratio to the second ideal effective length-to-width ratio is one because the cited limitations have been cited in claim 21 for the range of between ninety percent and one hundred and ten percent. Clarification is necessary.

Claims 6, 12, and 30 recite the limitation "the third resistor" in line 6. There is insufficient antecedent basis for this limitation in the claims.

Claim 29 recites the limitation "the first ideal effective length-to-width ratio" in line 4. There is insufficient antecedent basis for this limitation in the claim.

The term "approximately equal" in claims 6, 12, 18, and 30, is a relative term which renders the claim indefinite. The term "approximately equal" is not defined by the claims, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

It is not clear if the cited third resistor in claim 19 is the same as the third cited resistor in claim 17 or not.

In claim 24, it is not clear of the cited arrangement of the first field effect transistor unit comprises a plurality of field effect transistors coupled in parallel between the first voltage supply and the first resistor.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-3, 5, 17, 23, 24, 28, 29, and 34 are rejected under 35 U.S.C. 102(e) as being anticipated by Fifield et al. (U. S. PAT. 6,667,633).

In claim 1, Fifield et al. teaches all claimed features in Fig. 2, a digitally controlled impedance driver circuit comprising the following: a first voltage supply (VDDQ) that is configured to carry a first voltage (3.3V) during operation; an input/output node (DQi) upon which the digital controlled impedance driver circuit (24) is to apply a signal during operation; a first finger (54_0, 64) comprising a first field effect transistor unit (54_0) having a first ideal effective length-to-width ratio (a fixed length to 120 μm of 54_0) and having a source terminal coupled to the first voltage supply (as shown), and further comprising a first resistor (64) coupled in series between a drain terminal of the first field effect transistor unit and the input/output node, the first resistor having a first ideal resistance (72 Ω); and a second finger (54_1, 62) comprising a second field effect transistor unit (54_1) having a second ideal effective length-to-width ratio (the fixed length to 240 μm of 54_1) and having a source terminal coupled to the first voltage supply (as shown), wherein the second ideal effective length-to-width ratio is smaller than the first ideal effective length-to-width ratio (the fixed length to 240 μm of 54_1 is smaller than the fixed

length to 120 μm of 54_0), the second finger further including a second resistor (62) coupled in series between a drain terminal of the second field effect transistor unit and the input/output node, the second resistor having a second ideal resistance (36 Ω) that is smaller than the first ideal resistance (72 Ω).

In claim 2, Fifield et al. further teaches the digitally controlled impedance driver circuit in accordance with claim 1,wherein the ratio of the second ideal resistance (36 Ω) to the first ideal resistance (72 Ω) is between sixty percent and one hundred and fifty percent (100% is between 60% and 150%) of the ratio of the second ideal effective length-to-width ratio (the fixed length to 240 μm of 54_1) to the first ideal effective length-to-width ratio (the fixed length to 120 μm of 54_0).

In claim 3, Fifield et al. further teaches the digitally controlled impedance driver circuit in accordance with claim 2 wherein the ratio of the second ideal effective length-to-width ratio to the first ideal effective length-to-width ratio is between forty percent and sixty percent (50% is between 40% and 60%).

In claim 5, Fifield et al. further teaches the digitally controlled impedance driver circuit in accordance with claim 1 wherein the ratio of the second ideal effective length-to-width ratio to the first ideal effective length-to-width ratio is between forty percent and sixty percent (50% is between 40% and 60%).

In claim 17, Fifield et al. further teaches the digitally controlled impedance driver circuit in accordance with claim 1, further comprising the following: a second voltage supply (VSSQ) that is configured to carry a second voltage (ground) during operation that is less than the first voltage, wherein the first and second field effect transistor units

are respectively first and second p-type field effect transistor units; wherein the first finger further comprises a first n-type field effect transistor unit (56_0) having a source terminal coupled to the second voltage supply and a third resistor (64, the third resistor and the first resistor are common) coupled in series between a drain terminal of the first n-type field effect transistor unit (56_0) and the input/output node (Dqi); and wherein the second finger further comprises a second n-type field effect transistor unit (56_1) having a source terminal coupled to the second voltage supply (VSSQ).

In claim 23, Fifield et al. further teaches the digitally controlled impedance driver circuit in accordance with claim 1, wherein the first field effect transistor unit comprises a single field effect transistor (54_0).

In claim 24, Fifield et al. further teaches the digitally controlled impedance driver circuit in accordance with claim 1, wherein the first field effect transistor unit comprises a plurality of field effect transistors coupled in parallel between the first voltage supply and the first resistor.

In claim 28, Fifield et al. teaches all claimed features in Fig. 2, a digitally controlled impedance driver circuit comprising the following: a first voltage supply (VDDQ) that is configured to carry a first voltage (3.3V) during operation; an input/output node (DQi) upon which the digital controlled impedance driver circuit (24) is to apply a signal during operation; a first finger (54_0, 64) comprising a first field effect transistor unit (54_0) having a first effective length-to-width ratio (a fixed length to 120 μm of 54_0) and having a source terminal coupled to the first voltage supply (as shown), and further comprising a first resistor (64) coupled in series between a drain terminal of the first field

effect transistor unit and the input/output node, the first resistor having a first resistance (72 Ω); and a second finger (54_1, 62) comprising a second field effect transistor unit (54_1) having a second effective length-to-width ratio (the fixed length to 240 μm of 54_1) and having a source terminal coupled to the first voltage supply (as shown), the second finger further including a second resistor (62) coupled in series between a drain terminal of the second field effect transistor unit and the input/output node, the second resistor having a second resistance (36 Ω) wherein the second effective length-to-width ratio to the first effective length-to-width ratio (the fixed length to 240 μm of 54_1 over the fixed length to 120 μm of 54_0 is 50% which is less than 60%).

In claim 29, Fifield et al. further teaches the digitally controlled impedance driver circuit in accordance with claim 28,wherein the ratio of the second resistance (36 Ω) to the first resistance (72 Ω) is between eighty percent and one hundred and tweenty percent (100% is between 80% and 120%) of the ratio of the second effective length-to-width ratio (the fixed length to 240 μm of 54_1) to the first effective length-to-width ratio (the fixed length to 120 μm of 54_0).

In claim 34, Fifield et al. further teaches the digitally controlled impedance driver circuit in accordance with claim 28, further comprising the following: a second voltage supply (VSSQ) that is configured to carry a second voltage (ground) during operation that is less than the first voltage, wherein the first and second field effect transistor units are respectively first and second p-type field effect transistor units; wherein the first finger further comprises a first n-type field effect transistor unit (56_0) having a source terminal coupled to the second voltage supply and a third resistor (64, the third resistor

and the first resistor are common) coupled in series between a drain terminal of the first n-type field effect transistor unit (56_0) and the input/output node (Dqi); and wherein the second finger further comprises a second n-type field effect transistor unit (56_1) having a source terminal coupled to the second voltage supply (VSSQ).

5. Claims 7-9, 11, 13-15, 20, 21, 24, and 31-33 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

6. Claims 25-27 and 35-37 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 38-40 appear to comprise allowable subject matter.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vibol Tan

Primary Examiner, AU 2819

VIBOL TAN
PRIMARY EXAMINER